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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,640	01/16/2004	Craig Chaiken	16356.841 (DC-05832)	1223

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HAYNES AND BOONE, LLP
901 MAIN STREET, SUITE 3100
DALLAS, TX 75202

EXAMINER	
CHANG, ERIC	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,640	CHAIKEN ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-7, 10-19 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,708,278 to Howard et al., in view of U.S. Patent 6,347,202 to Shishizuka et al.

4. As to claim 1, Howard discloses a method for allowing a processor to enter low power states in an information handling system (IHS), the method comprising: in response to detecting that a bus mastering device is not needed, suspending a bus mastering device controller [col. 3, lines 34-45], wherein the now suspended controller no longer prevents the processor from entering low power states [col. 6, lines 42-62].

Howard teaches the limitations of the claim, but does not teach that detection that a bus mastering device is not needed is performed by failing to detect an access request for the bus mastering device within a predetermined period of time.

Shishizuka teaches a bus that can enter a low power state [FIG. 88], similar to that of Howard. Shishizuka further teaches detecting an access request for a bus device [FIG. 88]; and in response to failing to detect an access request for the bus mastering device within a predetermined period of time, suspending a bus device [FIG. 88].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the access request time-out to place the bus in a low power mode as taught by Shishizuka. One of ordinary skill in the art would have been motivated to do so to determine if a bus device is needed.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of conserving power in a bus system. Moreover, the access request time-out means taught by Shishizuka would improve the efficiency of Howard because it specifically teaches that a bus mastering device controller can be suspended when it is not needed because no access requests have occurred within a predetermined period of time.

5. As to claim 2, Shishizuka discloses starting a timer for the predetermined period of time [FIG. 88]; and in response to failing to detect an access request for the period of time, expiring the timer, wherein suspending the bus device is performed in response to the timer expiring [FIG. 88]. Howard teaches that a bus mastering device controller can be suspended if it is not needed [col. 3, lines 34-45]; it would be obvious to one of ordinary skill in the art that a bus device is not needed when no access requests have occurred.

6. As to claim 3, Shishizuka discloses in response to detecting an access request for the bus mastering device, restarting the timer for the predetermined period of time [FIG. 88].

7. As to claim 4, Shishizuka discloses in response to detecting an access request for the bus mastering device, also resuming operation of the bus device if the bus mastering device controller has been suspended [FIG. 88].

8. As to claim 5, Shishizuka discloses detecting an access request for the bus mastering device includes detecting an input/output request packet (IRP) [FIG. 88].

9. As to claims 6-7, Shishizuka discloses detecting an access request for the bus mastering device, starting the timer for the predetermined period of time, and resuming the operation of the bus device are performed in response to an executable code executable by the IHS [FIG. 88]. Furthermore, it is well known in the art that a filter driver is executable code used to control hardware devices within a computer system.

10. As to claims 10-13, Howard discloses the system comprises a bus mastering device for a USB bus [FIG. 2]. In addition, Shishizuka teaches that a bus in a computer system may be a USB [FIG. 4]. Furthermore, USB bus devices such as a floppy disk drive and an optical disk drive are well known in the art.

11. As to claim 14, Howard discloses an information handling system (IHS) comprising: a processor [202] capable of entering low power states, a memory coupled to the processor [204]; a non-volatile storage, coupled to the processor [206]; a bus mastering device [120]; a bus mastering device controller coupled to the bus mastering device and the processor, for

transferring information between the bus mastering device and the processor [212]; and an executable code stored in the non-volatile storage for suspending the bus mastering device controller if it is not needed [col. 3, lines 34-45]. Shishizuka discloses starting a timer for the predetermined period of time [FIG. 88]; and in response to failing to detect an access request for the period of time, expiring the timer, wherein suspending the bus device is performed in response to the timer expiring [FIG. 88]. It would be obvious to one of ordinary skill in the art that a bus device is not needed when no access requests have occurred, and therefore may be suspended.

12. As to claim 15, Shishizuka discloses the executable code starts a timer for the predetermined period of time, expires the timer in response to failing to detect an access request for the bus mastering device within the time period, and wherein causing the bus device to be suspended is in response to the timer expiring [FIG. 88].

13. As to claim 16, Shishizuka discloses the executable code restarts the timer for the predetermined period of time in response to detecting an access request for the bus mastering device [FIG. 88].

14. As to claim 17, Shishizuka discloses the executable code further causes the bus device to resume operation in response to detecting an access request for the bus device, if the bus device has been suspended [FIG. 88].

15. As to claim 18, Shishizuka discloses detecting an access request for the bus mastering device includes detecting an input/output request packet (IRP) [FIG. 88].

16. As to claim 19, Shishizuka discloses detecting an access request for the bus device, starting the timer for the predetermined period of time, and resuming the operation of the bus device are performed in response to an executable code executable by the IHS [FIG. 88]. Furthermore, it is well known in the art that a filter driver is executable code used to control hardware devices within a computer system.

17. As to claims 22-25, Howard discloses the system comprises a bus mastering device for a USB bus [FIG. 2]. In addition, Shishizuka teaches that a bus in a computer system may be a USB [FIG. 4]. Furthermore, USB bus devices such as a floppy disk drive and an optical disk drive are well known in the art.

18. As to claim 26, Howard discloses an information handling system (IHS) comprising: a processor [202] capable of entering low power states, a memory coupled to the processor [204]; a non-volatile storage, coupled to the processor [206]; a bus mastering device [120]; a bus mastering device controller coupled to the bus mastering device and the processor, for transferring information between the bus mastering device and the processor [212]; and means for suspending the bus mastering device controller if it is not needed [col. 3, lines 34-45]. Shishizuka discloses starting a timer for the predetermined period of time [FIG. 88]; and in response to failing to detect an access request for the period of time, expiring the timer, wherein

suspending the bus device is performed in response to the timer expiring [FIG. 88]. It would be obvious to one of ordinary skill in the art that a bus device is not needed when no access requests have occurred, and therefore may be suspended.

19. As to claim 27, Howard discloses an information handling system (IHS) comprising: a processor [202] capable of entering low power states, a memory coupled to the processor [204]; a non-volatile storage, coupled to the processor [206]; a bus mastering device [120]; a bus mastering device controller coupled to the bus mastering device and the processor, for transferring information between the bus mastering device and the processor [212]; and storing means for suspending the bus mastering device controller if it is not needed [col. 3, lines 34-45]. Shishizuka discloses starting a timer for the predetermined period of time [FIG. 88]; and in response to failing to detect an access request for the period of time, expiring the timer, wherein suspending the bus device is performed in response to the timer expiring [FIG. 88]. It would be obvious to one of ordinary skill in the art that a bus device is not needed when no access requests have occurred, and therefore may be suspended

20. Claims 8-9 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,708,278 to Howard et al., in view of U.S. Patent 6,347,202 to Shishizuka et al., in further view of Applicant's Admitted Prior Art.

21. As to claims 8-9, Shishizuka discloses in conjunction with suspending the bus mastering device controller, setting a flag indicating that the bus device has been suspended in response to

the IHS executing the executable code [FIG. 88]; and resuming operation of the bus device if the flag is set [FIG. 88]. In addition, Applicant's Admitted Prior art teaches that the ACPI standard is well known in the art [paragraph 0003]. The ACPI standard further comprises use of flags to indicate power states of devices, as well as SMI protocols.

22. As to claims 20-21, Shishizuka discloses in conjunction with suspending the bus device, setting a flag indicating that the bus device has been suspended in response to the IHS executing the executable code [FIG. 88]; and resuming operation of the bus device if the flag is set [FIG. 88]. In addition, Applicant's Admitted Prior art teaches that the ACPI standard is well known in the art. The ACPI standard further comprises use of flags to indicate power states of devices, as well as SMI protocols.

Response to Arguments

23. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 12, 2007
ec

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/16/07